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Performance Study of NOC Virtual Channel Router Architecture

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Abstract*—Thenetwork-on-chip (NOC) has been proposed for system-on–chip (SOC) based applications to achieve the better performance with low power consumption as compaired with typical on-chip bus architecture.Power consumption can be decreased by reducing the size of the router buffers. However, as reducing router buffers alone will significantly reduces performance, we compensate by utilizing the newly proposed dual-function virtual channel buffers that allow flits to be stored on wires when required.This paper presents a novel virtual-channel (VC) sharing technique for NOC architecture. The proposed architecture improves the utilization of resources to enhance the performance with minimal overheads. Resource sharing for on-chip network is critical toreduce the chip area and power consumption. Thus virtual channel buffer sharing by other router ports has been proposed to enhance the performance of on-chip communication.*

In this paper, we proposed the router architecture optimization by utilizing the ideal buffer instead of increasing number and size of buffers for desired area and power requirement results.

***IndexTerms*—Networks-on-Chip (NOC), Virtual Channel (VC), Processing Element Recovery (PE),Partial Virtual Channel Sharing (PVC).**

I. INTRODUCTION

Atypical NOC based system consists of processing elements (PE), network interfaces (NI), routers and channels. The router further contains switch, buffers and routing logic as shown in Figure 1. Buffers consume nearabout 64% of the total node (router + link) leakage power for all process technologies, which makes it the largest power consumer in any NOC system. All links in NOC can be simultaneously used for data transmission, which provides a high level of parallelism. It is an attractive solution to replace the conventional communication architectures such as shared buses or point-to-point dedicated links by NOC. NOC provides better scalability than on-chip buses because as more resources are introduced to a system, also more routers and links are introduced to connect them to the network [4]. Buffers consume the largest fraction of dynamic and leakage power of the NOC node (router + link) [3]. Storing a packet in buffer consumes far more power as compared to its transmission [3]. Thus, increasing the utilization of buffers and reduction in their number and size with efficient autonomic control reduces the area and power consumption. Also the Wormhole flow control [2] has been proposed to reduce the buffer requirements and enhance the system throughput.

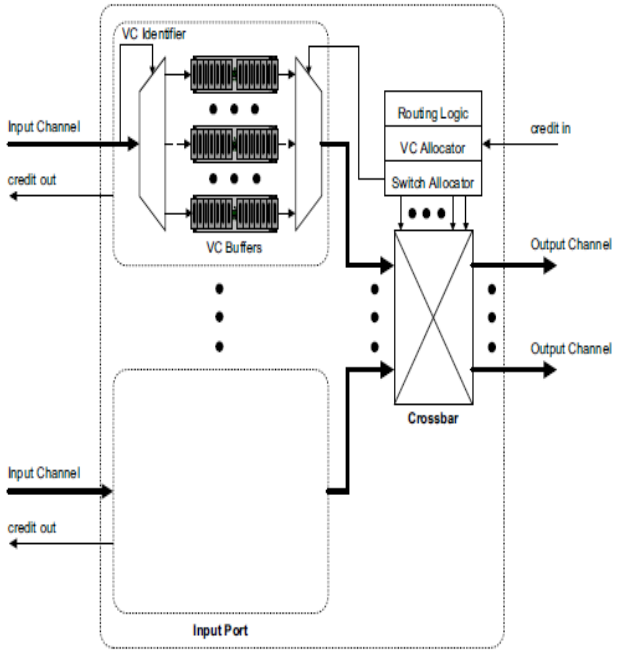

Figure 1.Conventional virtual channel router architecture.

However, one packet may be occupy or cover several intermediate switches at the same time. This introduces the problemof deadlocks and livelocks [8]. Thus to avoid this problem the use of virtual channel is introduced. Virtual channel flow control exploits an array of buffers at each input port. By allocating different packets to each of these buffers, flits from multiple packets may be sent in an

interleaved manner over a single physical channel. This improves the throughput and reduces the average packet latency.

II. RELATED WORK

Buffer management is not a recent issue but still needs attention. This comes as a performance improvement to utilize the unused buffers at some time instant. Lately, buffer sharing has been analyzed and compared to the existing router architectures.[1]This paper proposed combine two techniques of adaptive channel buffers and router pipeline bypassing to simultaneously reduce power consumption and improve performance.This paper simulation results of the proposed methodology combining the two techniques, yield a overall power reduction of 62% over the baseline and improve performance (throughput and latency) by more than 10%.

Increasing the utilization of buffers and reduction in their number and size with efficient autonomic control reduces the area and power consumption. In this paper, Wormhole flow control has been proposed to reduce the buffer requirements and enhance the system throughput[4].

Lan et. al [6] addresses the buffer utilization by making the channels bidirectional and shows significant improvement in system performance. But in this case, each channel controller has two additional tasks: dynamically configuring the channel direction and to allocate the channel to one of the routers, sharing the channel. Also, there is a 40% area overhead over the typical NOC router architecture due to double crossbar design and control logic. The extra tasks for channel controller and increased crossbar size contribute to the power consumption as well

Nicopoulos et al.[9] presents a Dynamic *Virtual ChannelRegulator* (ViChaR) for NOC routers. The authors address the buffer utilization by using the unified buffered structure (UBS) instead of individual and statically partitioned FIFO buffers. It provides each individual router port with a variable number of VCs according to the traffic load. The architecture provides around 25% improvement in system performance at a small cost of power consumption. The architecture enhances the buffer utilization under heavy traffic load at the port. If there is no load at the port, the buffer resources cannot be utilized by other loaded ports.

Ramanujamet. al [10] introduces a distributed shared buffer (DSB) NOC router architecture. The proposed architecture shows a significant improvement in throughput at the expense of area and power consumption due to extra crossbar and complex arbitration scheme.

Kodiet. al [11] illustrates the impact of repeater insertion on inter-router links with adaptive control and eliminating some of the buffers in the router. The approach saves appreciable amount of power and area without significant degradation in the throughput and latency. But there is still some scope to increase the buffer utilization inside the router by using the architecture which we propose here.

The main motivation of this work is to propose a NOC architecture with considerations of all the issues discussed above. A NOC architecture with an ideal tradeoff between the performance and the mentioned issues guides to propose the partial sharing of VC buffers.

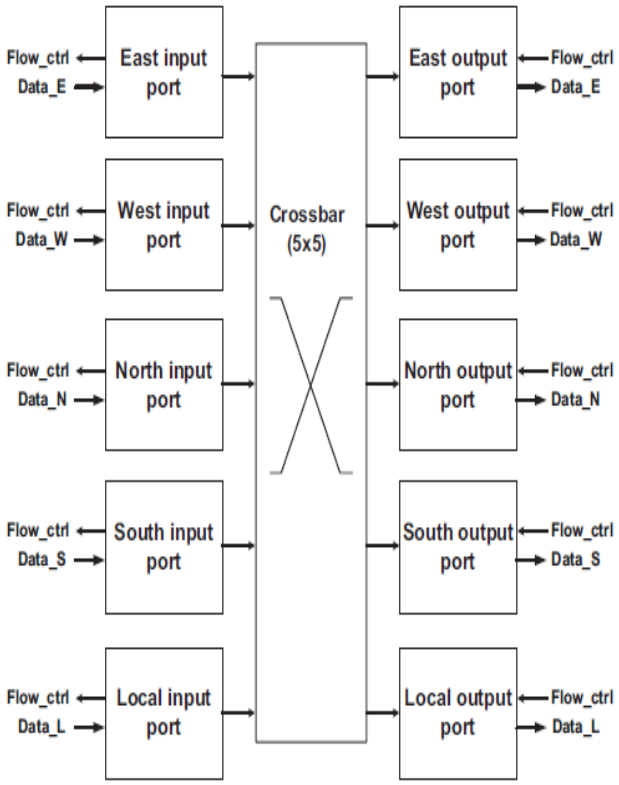

Figure.2.Base router architecture

The drawback of using VCs stands in a more complexcontrol protocol, as data corresponding to different messages which is multiplexed on the physical channel must be eventually separated [8]. Another important issue that needs attention is the utilization tradeoff. VCs are proposed to increase the utilization of physical channels. By inserting the VC buffers, we increase the physical channel utilization but utilization of inserted VC buffers is not considered. It can be observed that if there is no communication on somechannel at some time instant and at the same time, neighboring channel is overloaded, free buffers of one channel cannot contribute for congestion control by sharing the load of neighboring channel.

III. PROPOSED ARCHITECTURE

To enhance the performance of typical VC architectures, new VC buffers should be inserted because a congested port

cannot utilize the resources of neighbouring free port. VC utilization can be enhanced by sharing free buffers of a port with neighbouring overloaded input ports. The improved VC utilization directs to reduce the number of VC buffers and sustain the system performance. VC utilization can be further improved by sharing them among all the input ports. However, full sharing increases the control logic complexity and power consumption due to a larger input crossbar. Thus a tradeoff between resource utilization, design complexity and power consumption is needed.

Instead of sharing the VC buffers among all the input ports, PVS approach shares the VC buffers among few input ports according to the communication requirements. With this technique, the buffer utilization is increased and utilization level approaches close to the fully shared architecture without significant silicon area and power consumption overhead because of reduced input crossbar size.

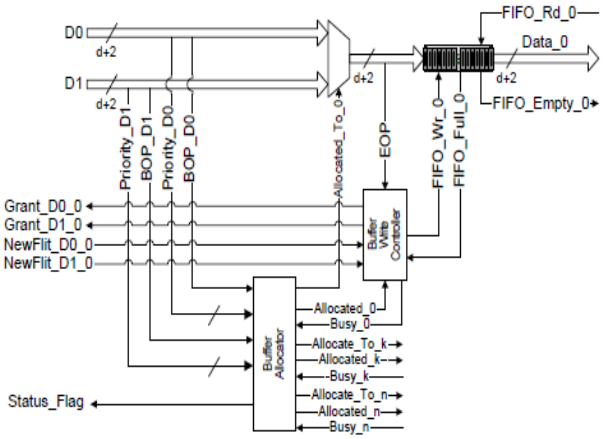

Figure 3. Proposed input part of router architecture

NI is a generic interface, which needs to be standardized. Main tasks of the NI are packetization and de-packetization of data. Different services can be introduced in NI architecture, such as multicasting and error monitoring. The queuing buffer for the PE can be considered as the part of NI on input port of the switch. Thus each PE has its own dedicated buffer, which simplifies the control logic and enhance the throughput without any area overhead. PI is the core specific interface, which acts as a clock synchronizer. In PVS approach, the input crossbars and control logicare responsible for buffer allocation and receiving the data packets. Input architecture uses the distributed routing logic where as central VC allocator is used for the group of channels sharing the buffers.

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The proposed architecture, sharing of buffers between neighbouring input ports, is shown in Fig.2. The router architecture can be divided into two parts, the Input and the Output. The Input part is responsible for buffer allocation and receiving the packets from neighbouring routers. The Output part computes the route and transmits the packets accordingly. Within the router, the Input and the Output parts do not communicate at all. Both parts simply write andread from the buffers. Fig.2 shows the signals of both parts to write and read from buffers and also the external interface of router.

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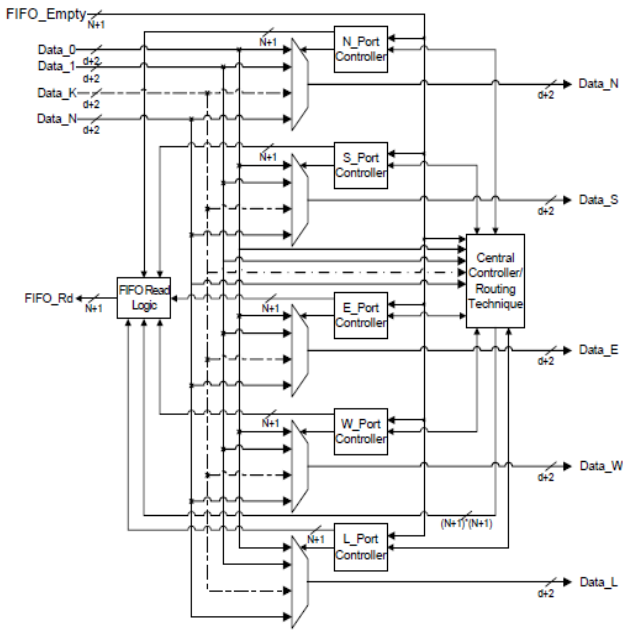

Figure 4. Proposed output part of router architecture

For two channels sharing the buffers, input PVS architecture is shown in Figure.3. The VC allocator for one group of channels sharing the buffers operates according to the buffers status and does not communicate with other VC allocators. The task of VC allocator is to keep track of free buffers and allocate them to the incoming traffic. After allocation, routing logic computes the route for the packet and selects the port on output crossbar for packet transmission. The routing logic is a fault tolerant approach because of distributed nature. If one routing element is faulty, only the corresponding buffers and channels are

affected. Distributed routing logics also reduce the communication overhead and power consumption.

IV. DISCUSSION

In typical NOC mesh, processing nodes can be dividedinto three different categories according to the position :corner, edge and central nodes. Routers on the basis of these categories require three, four and five I/O ports respectively. Because of the distributed and independent control logic, router can be configured to fulfil these requirements without any extra effort by simply removing the extra hardware. Thus the architecture is fully optimized for any number of I/O ports. The number of I/O ports can be increased to any number by simply duplicating the hardware on input side and increasing the crossbar size on output side. At the same time, the buffer utilization is increased which significantly reduces the new buffer requirements. Thus decreasing the buffer size by 4 buffer slots (25%) leads to a power savings of 25.72% as compared to the baseline. Power reduces by 40.77% when the buffer size is reduced to 50% of the baseline[3].The proposed architecture can be integrated into the existing automated NOC design flow without requiring extra effort. An automated design flow can utilize the adoptability feature of this architecture to generate an optimized router module according to the application and design requirements. Therefore, the proposed architecture can play a significant role in maintaining the performance of NOC based systems regardless of the topology.

V. CONCLUSIONS AND FUTURE WORKS

Thus we are going to see a similar approach that can be taken for the further development of NOC systems, in order to raise the level of abstraction towards application layers.A very important step is to utilize the buffers for routing purposes within the cluster without injecting the packets to the network. It will help to compensate the overheads and enhance the system performance. Apart from presented results, power consumption analysis and realistic traffic analysis are future topics for analysis and implementation for the proposed router architecture.

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